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APPLICATION FOR UNITED STATES LETTERS PATENT

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FOR: METHOD FOR SLOWING DOWN DOPANT-ENHANCED DIFFUSION IN SUBSTRATES AND DEVICES FABRICATED THEREFROM

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METHOD FOR SLOWING DOWN DOPANT-ENHANCED DIFFUSION SUBSTRATES AND DEVICES FABRICATED THEREFROM

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to a semiconductor device, and more particularly to a method and structure for slowing down dopant diffusion in strained Si/Ge substrates for junction formation for devices (e.g., N-MOS devices) in strained Si/SiGe substrates.

Description of the Related Art

Strained Si complementary metal oxide semiconductor (CMOS) devices with a strained Si channel on a relaxed $Si_{1-x}Ge_x$ buffer layer offer better device performance over conventional Si CMOS because of the enhancement in both channel electron and hole mobilities, and have been demonstrated for devices as small as about 60 nm (e.g., see Figure 1 showing a structure 100 including a gate 110, an oxide spacers 120 formed on each side of the gate 110, and an extension junction region 130 formed in the vicinity of the oxide spacer 110).

However, for devices with L_{eff} at about 60 nm or below, an extension junction depth Xj ~ 30 nm or below would be needed. The diffusion of a dopant in SiGe can form parasitic barriers at the heterojunction in a heterojunction bipolar transistor (HBT).

More importantly, the junction slope Xjs near the channel region should be abrupt (< 6 nm/decade), and the dopant concentration at the extension 130 should be ~ 1E20/cm^3.

However, the present inventors have recognized that these shallow junction requirements are difficult to achieve for a dopant (e.g., arsenic) junction in N-type metal oxide semiconductor (NMOS) devices in strained $Si/Si_{1-x}Ge_x$ substrates due to significant arsenic-enhanced diffusion.

That is, experimentally, it has been found that arsenic dopant diffusivity increases exponentially with the percentage of the Ge content in the $Si_{1-x}Ge_x$ buffer layer.

Thus, the present inventors have recognized that this enhanced arsenic dopant diffusion in strained $Si/Si_{1-x}Ge_x$ substrates becomes a significant roadblock for generating ultra-shallow junctions for a small (e.g., about sub-50 nm) NMOS device in strained Si substrates where high %Ge (e.g., > about 20%) is used for higher electron and hole mobility for improved device performance.

In addition, for a sub-50 nm device, the enhanced lateral arsenic dopant diffusion will short-circuit (e.g., see Figure 1) the source and drain regions of the NMOS device, and will render the device totally inoperable.

That is, as shown in Figure 1, arsenic dopant concentration at about 1E19/cm^3 and about 1E19cm^3 are immediately below the center of the gate 110 (e.g., a polysilicon gate). This high concentration of dopant underneath the gate indicates shorting due to enhanced arsenic junction diffusion from the extension junction region 130 to the gate region 110.

Thus, the present inventors have recognized that, prior to the present invention, there have been no known techniques (or resulting structures) for slowing down the arsenic enhanced diffusion in strained $Si/Si_{1-x}Ge_x$ or $Si_{1-x}Ge_x/Si$ device substrates.

SUMMARY OF THE INVENTION

In view of the foregoing and other problems, drawbacks, and disadvantages of the conventional methods and structures, an exemplary feature of the present invention is to provide a method and structure for slowing down the dopant (e.g., arsenic, P, and/or Sb) enhanced diffusion in strained $Si/Si_{1-x}Ge_x$ device substrates.

An exemplary aspect of the present invention includes a method of forming a semiconductor device. The method includes implanting, on a substrate, a dopant and at least one species, and annealing the substrate, the at least one species retarding a diffusion of the dopant during the annealing of the substrate.

Specifically, the dosage of the at least one species may exceed a preamorphization threshold of the substrate. In particular, a dosage of the at

least one species is at least about 3 times the preamorphization threshold of the substrate, and in some cases, the dosage of the at least one species is at least about 5 times the preamorphization threshold of the substrate, or at least about 7 times the preamorphization threshold of the substrate.

Further, the at least one species may damage a junction (e.g., an extension junction) formed by the dopant. For example, the junction may have a thickness of no more than about 30 nm. Further, the junction may have a slope which is at least about 5 nm per decade of change in concentration of the dopant.

Further, the substrate may include one of silicon, SiGe, and strained Si. In addition, the at least one species may include at least one of Xe, Ge, Si, Ar, Kr, Ne, He and N, and the dopant may include at least one of As, P, and Sb. In addition, the dopant may be implanted at a time which is one of prior to the implanting the species, and after the implanting of the species.

The method may also include forming a source and drain region in the substrate, and forming a metal silicide contact over the source and drain region. For example, the source and drain region may be formed at a time which is prior to the implanting of the dopant, or after the implanting of the dopant. In any case, the dopant may be implanted at a time which is one of prior to the implanting the species, and after the implanting the species.

Further, the species may be implanted at least about 10 to about 20 nm deeper than the dopant. In addition, the species may have an implantation energy for surrounding at least a portion of an extension region in the

substrate. In addition, the species may have a first implantation energy for sufficient to create a region surrounding at least a portion of an extension region in the substrate, and a second implantation energy (e.g., greater than the first implantation energy) sufficient to create a region for surrounding at least a portion of a source/drain region in the substrate. The species may alternatively have an implantation energy sufficient for creating a region for surrounding at least a portion of an extension region and at least a portion of a source/drain region in the substrate.

Another aspect of the present invention includes a method of reducing a thermal diffusion of a dopant. The method includes implanting a dopant on a substrate, implanting, as a second species with the dopant, at least one species on the substrate, and annealing the substrate, the at least one species retarding a diffusion of the dopant during the annealing of the substrate.

For example, the annealing the substrate may be performed after the implanting the dopant and the implanting the species. Further, the implanting the dopant may be performed after the implanting the at least one species. In that case, the method may further include annealing the substrate after the implanting the species and before the implanting the dopant.

Another aspect of the present invention includes a method of forming a junction in a semiconductor substrate. The method includes implanting a dopant on a substrate, implanting, as a second species with the dopant, at least one species on the substrate, and annealing the substrate, the at least one

species retarding a diffusion of the dopant during the annealing of the substrate.

Another aspect of the present invention includes a semiconductor device, which includes a semiconductor substrate, a dopant formed in the substrate, to define a junction, and a species formed in the substrate as a second species with the dopant, and in a concentration which is sufficient to retard a diffusion of the dopant. The device may further include a gate formed over the channel, a source and drain region formed adjacent the first and second materials, and a contact formed over the source and drain regions.

For example, the junction may have a thickness of no more than about 30 nm, and a slope which is at least about 5 nm per decade of change in concentration of dopant. Further, the substrate may include one of silicon, SiGe, and strained Si. For example, the SiGe may include one of relaxed SiGe and strained SiGe. Further, the strained SiGe may include SiGe under one of a compressive strain and a tensile strain.

Hence, with the unique and unobvious combination of exemplary features of the invention, the present invention provides a method and structure for slowing down the arsenic enhanced diffusion in strained $Si/Si_{1-x}Ge_x$ device substrates. The invention can also be extended to silicon substrates and strained $Si_{1-x}Ge_x/Si$.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other exemplary purposes, aspects and advantages will be better understood from the following detailed description of exemplary embodiments of the invention with reference to the drawings, in which:

Figure 1 shows a graph (and structure 100) which illustrates that as arsenic dopant concentration increases, shorting due to enhanced arsenic junction diffusion from an extension junction region 130 to a gate region 110 may occur;

Figure 2 illustrates a structure 200 formed according to an exemplary embodiment of the present invention;

Figure 3A illustrates a comparison of arsenic junction profiles with (and without) an atom/ion species (e.g., Xe, Si, etc.) according to an exemplary technique of the present invention;

Figure 3B illustrates a profile of a junction formed according to an exemplary aspect of the present invention;

Figures 4A-4D illustrate processing steps of a first exemplary technique of forming a CMOS (e.g., NMOS) device according to the present invention;

Figure 4E illustrates a flowchart 400 of the exemplary technique of Figures 4A-4D;

Figure 5A-5D illustrate processing steps of a second exemplary technique of forming a CMOS (e.g., NMOS) device according to the present invention;

Figure 5E illustrates a flowchart 500 of the exemplary technique of Figures 5A-5D;

Figures 6A-6D illustrate processing steps of a third exemplary technique of forming a CMOS (e.g., NMOS) device according to the present invention;

Figure 6E illustrates a flowchart 600 of the exemplary technique of Figures 6A-6D;

Figures 7A-7F illustrate processing steps of a fourth exemplary technique of forming a CMOS (e.g., NMOS) device according to the present invention; and

Figure 7G illustrates a flowchart 700 of the exemplary technique of Figures 7A-7F.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS OF THE INVENTION

Referring now to the drawings, and more particularly to Figures 2-7G, there are shown exemplary embodiments of the method and structures according to the present invention.

EXEMPLARY EMBODIMENT

Generally, the exemplary techniques according to the present invention advantageously use the implanting of at least one atom/ion species (e.g., one

or a plurality of atom/ion species) on a substrate. For example, the atom/ion species may include an inert species (e.g., Xe, Ge, Si, Ar, Kr, Ne, He, and N) and may be implanted in a vicinity of a device dopant (e.g., arsenic will be assumed throughout the present application, but as mentioned above the dopant may be P, and/or Sb). Specifically, the atom/ion species may be implanted in the vicinity of an extension region (e.g., an extension junction region) and/or a source/drain region (e.g., a source/drain junction region) of the substrate (e.g., a strained $Si/Si_{1-x}Ge_x$ substrate).

Specifically, the present inventors have discovered that the excess interstitials and vacancy sinks created by the atom/ion species in the vicinity of the arsenic dopants help to slow down both vertical and lateral arsenic enhanced diffusion in the extension junction region or both the arsenic extension or source/drain junction regions.

Thus, the method of the present invention enables sub-30 nm (e.g., junction depths in a range of about 20 nm to about 30 nm have been shown by the present invention), ultra-shallow arsenic junction to be formed in the strained $Si/Si_{1-x}Ge_x$ substrate, and prevents undesirable lateral arsenic diffusion into the device channel region.

In this manner, the present invention enables high performance sub-50 nm NMOS devices to be fabricated in strained $Si/Si_{1-x}Ge_x$ substrates. It is noted that the strained substrates could be under tensile or compressive strain. By the same token, the SiGe could be relaxed. There is no requirement that it be strained.

Turning now to Figure 2, Figure 2 illustrates a structure 200 formed by the present invention. As shown, the structure (e.g., an exemplary NMOS device) 200 includes a substrate 210 (e.g., preferably formed of silicon or the like), a relaxed Si_{1-x}/Ge_x layer 220 formed over (e.g., on top of) the Si substrate 210. The Si/Ge layer 220 is a graded layer which has a crystal lattice which is more and more relaxed in a direction extending away from a top surface of the substrate 210 with the concentration of Ge increasing in a direction away from the top surface of the substrate 210.

A relatively inert atom/ion species (e.g., Xe, Ge, Si, Ar, Kr, Ne, He, and N) 230 implant is formed below an arsenic extension 240, and is formed to surround first and second surfaces of the arsenic extension 240 (e.g., unreferenced; in Figure 2, a bottom surface and a side surface of the arsenic extension 240).

Additionally, preferably, the atom/ion species selected is from other than the dopant being employed (e.g., in the present exemplarily application, the atom/ion species is preferably selected to be other than the As dopant).

A strained silicon channel 250 is formed between opposing side surfaces of adjacent arsenic extensions 240, which have the atom/ion species thereon.

A gate 270 (e.g., formed of polysilicon, metal or the like) is formed above the strained silicon channel 250. A gate oxide 260 is formed between the gate 270 and the channel 250. A shallow trench isolation (STI) 290,

formed of dielectric or the like, is formed between devices, adjacent the source and drain.

Thus, as illustrated exemplary in Figure 2, after the implant of arsenic dopants in the extension regions 240, the atom/ion species (e.g., Xe, Si, etc.) implant species are implanted around (e.g., around at least a portion of) the arsenic extension junction region of the NMOS device in strained $Si/Si_{1-x}Ge_x$ substrates.

The implant range of the Xe or Si is such that it is about 10 to about 20 nm deeper than that of the arsenic dopant as implant depth, such that the Xe or Si atom/ion implant species create excess interstitials and vacancy sinks, thereby to reduce the vacancy population in the immediate vicinity of the arsenic dopants during annealing of junctions of the arsenic extensions 240.

In this manner, the arsenic dopant diffusion is greatly reduced, and enables much shallower arsenic junctions to be formed in NMOS devices in strained $Si/Si_{1-x}Ge_x$ substrates.

Thus, the mechanism of enhanced Arsenic diffusion in strained $Si/Si_{1-x}Ge_x$ with %Ge > 20% is largely due to high vacancy population in the $Si_{1-x}Ge_x$ layer and the corresponding increase in the vacancy component of arsenic diffusion.

As mentioned above, an exemplary aspect of the present invention is using implanting of atom/ion species (e.g., Xe, Ge, Si, Ar, Kr, Ne, He, and N) in the device extension junction region or arsenic device extension and source drain junction regions in the strained $Si/Si_{1-x}Ge_x$ substrate.

It is noted that the present invention is not limited to the above species, but any species may be used so long as the species retards a diffusion of the dopant (e.g., arsenic in the exemplary embodiment, but the dopant may also include, for example, P, and/or Sb) in the substrate. Further, it is preferable generally that the atomic/ionic species be larger rather than smaller.

During rapid thermal anneal (RTA), the excess interstitials and vacancy sinks created by the atom/ion species help to reduce the vacancy population, and hence retard the arsenic diffusion in the strained $Si/Si_{1-x}Ge_x$ substrates.

An example of slowing down arsenic junction diffusion in strained $Si/Si_{1-x}Ge_x$ substrates along section A-A' in Figure 2 is demonstrated in the comparison of arsenic dopant junction profiles shown in Figure 3A for the cases of with, or without, Xe or Si as a second species implanted with the arsenic extension junction.

That is, Figure 3A illustrates experimental data (SIMS profiles) which shows the slow down of As dopants diffusion in strained $Si/Si_{1-x}Ge_x$ with Xe or Si species implants. In these experiments, a 50-nm, low temperature oxide (LTO) was formed on strained $Si/Si_{1-x}Ge_x$ with a 5 nm silicon cap, with X =30%.

That is, in these examples, the strained Si cap thickness was ~ 5 nm, the Ge content in the $Si_{1-x}Ge_x$ relaxed buffered layer is ~ 30%, the arsenic junction implant was about 1 kV with about 1E15/cm^2 dose, the Xe or Si second species was such that their implant range was ~ 10 nm deeper than the

1 kV arsenic as implant range. The implant dosage for the Xe or Si second species was about 5E14/cm^2 or about 5E15/cm^2, respectively.

These dosages are advantageously above (e.g., preferably far above) the preamorphization threshold dosage for the atom/ion species (e.g., Xe and Si species), such that a sufficient amount of excess interstitials and vacancies sinks are generated to slow down arsenic dopant motions.

That is, for purposes of the present application, "preamorphization threshold" means the dosage at which a crystal lattice converts into a substantially completely random (e.g., "damaged") pattern, thereby to become an amorphous structure.

Thus, whichever atom/species is used, the dosage should be above (e.g., preferably far above) the preamorphization threshold to enable such a conversion. As would be known by one of ordinary skill in the art taking the present application as a whole, the preamorphization threshold will vary depending upon which species/atom is employed. A larger atom will create more damage (e.g., excess interstitials and vacancy sinks, etc.), and thus a smaller total dosage can be employed.

Conversely, a smaller atom will create relatively less damage, and thus will use a larger dosage, to achieve the preamorphization threshold. Hence, whatever atom is employed, a dosage is selected which is above (e.g., preferably at least about 3 times above, and in many cases more preferably, at least about 5 times above, and most preferably at least about 7 times above) the dosage to meet the preamorphization threshold.

Thus, for example, for Xenon, the preamorphization threshold dosage is approximately 1E14/cm^2. Thus, the dosage for Xenon could be at least about 3E14/cm^2 (e.g., about 3E14/cm^2 to about 5E14/cm^2). Further, for silicon, the preamorphization threshold dosage is approximately 1E15/cm^2. Thus, the dosage for silicon could be at least about 3E15/cm^2 (e.g., about 3E15/cm^2 to about 5E15/cm^2).

Again, it is noted that the invention can be generalized to using an implant species using an exemplary dosage to cause damage resulting in interstitials and vacancy sinks which would slow down the dopant mobility.

Additionally, the implant species preferably is formed relatively near the vicinity of the junction implant (e.g., arsenic in the exemplary case). Thus, for example, the implant species (e.g., Xe, Si, etc.) can be within about 100 Å to about 200 Å from the As junction implant profile.

That is, suppose the As junction profile is upwards of about 100 Å, then the peak of the species (e.g., Xe) can be implanted at about the 100 Å region or about the 300 Å region (e.g., right behind it).

Then, the arsenic junction and the Xe (or Si or other species) co-implants are annealed rapidly together in a range preferably within about 800 to about 1100 °C for about 1 second to about 5 seconds, for implant damage removal and dopant activation.

For such an anneal, a rapid thermal anneal (RTA) (or "spike annealing") may be employed in a which a high temperature (e.g., about 1100 °C) is immediately obtained in a very short time period (e.g., the short period

of time being defined and limited in practice to what the specific RTA tool can achieve). For such an RTA or "spike annealing", a flash lamp (e.g., halogen lamp, laser light, etc.) could be employed. In the examples of Figure 3A, RTA conditions were 1000 °C/1s in 100% argon.

As shown in Figure 3A, with an ultra-high chemical vapor deposition (UHCVD) strained $Si/Si_{1-x}Ge_x$ (x = 20%) in a comparison with the As junction with no second species implanted (e.g., Xe, Si, etc.), there was a significant reduction in arsenic junction diffusion with a Xe or Si species implant, whereas without a Xe or Si species implant, the arsenic junction depth at $1E18/cm^3$ dopant concentration was ~ 85 nm. With a Xe species, As junction depth was ~ 30 nm. With a Si species implant, the As junction was ~ 50 nm.

Thus, this example demonstrates the Xe species implants can reduce the Arsenic junction depth (e.g., by almost a factor of 3). The arsenic shallow junction depth of about 30 nm achieved with species (e.g., Xe, Si, etc.) co-implants enables high performance sub-50 nm NMOS device to be fabricated in the strained $Si/ Si_{1-x}Ge_x$ substrates.

For example, Figure 3B illustrates the arsenic junction profiles for two junctions formed with and without a Xe species implant employed in a structure including the ultra-high chemical vapor deposition (UHCVD) strained $Si/Si_{1-x}Ge_x$ (x = 20%). A Si cap about 20 nm was also employed, and the RTA conditions were 1000 °C/5s in 100 % argon.

It is understood that the quality of a junction may be defined by the shallowness of the junction and the abruptness (e.g., the sharpness of the

slope) of the junction. Figure 3B illustrates such an improved quality junction, and specifically a junction with Xe species implant having a depth of about 20 nm and a slope of about 5 nm per decade of change in concentration of dopant (e.g., in a vicinity of the junction), which is much improved over conventional junctions.

Hereinbelow and referring to Figures 4A-7G, various exemplary process flows are described for the generation of high performance sub-50 nm NMOS device in strained $Si/Si_{1-x}Ge_x$ substrates incorporating the exemplary method of the present invention.

First Exemplary Technique

Figures 4A-4D illustrate processing steps of a first exemplary technique of forming a CMOS (e.g., NMOS) device according to the present invention. Figure 4E illustrates a flowchart 400 of the exemplary technique of Figures 4A-4D.

First, in Figure 4A and as shown in Figure 4E, in step 410, an arsenic extension implant 440 is formed. As shown, the implant 440 is formed in a structure 400 somewhat similar to structure 200 shown in Figure 2.

That is, structure 400 includes a substrate 410 (e.g., preferably formed of silicon, silicon-on-insulator (SOI), or the like), and a relaxed Si_{1-x}/Ge_x layer 420 formed over (e.g., on top of) the substrate 410. The Si/Ge layer 420 is a graded layer which has a crystal lattice which is more and more relaxed in a direction away from a top surface of the substrate 410, as a result of the Ge

concentration in the Si/Ge layer increasing in a direction going away from the top surface of the substrate 410.

A strained silicon channel 450 is formed between opposing side surfaces of adjacent arsenic extensions 440.

A gate 470 (e.g., formed of polysilicon, metal or the like) is formed above the stained silicon channel 450. A gate oxide 460 is formed between the gate 470 and the channel 450. A shallow trench isolation (STI) 490, formed of dielectric or the like, is formed between devices, adjacent the source and drain.

As illustrated in Figure 4B, after the implant of arsenic dopants in the extension regions 440, the atom/ion species (e.g., Xe, Si, etc.) are implanted around (e.g., around at least a portion of) the arsenic extension junction 440 region of the NMOS device in strained $Si/Si_{1-x}Ge_x$ substrates. (In this exemplary application, Xe or Si will be assumed to have been used.)

In Figure 4B (and as shown in Figure 4E, in step 420), the atom/ion species (Xe, Ge, Si, Ar, Kr, Ne, He, and N) implant 430 is formed, as described above. As shown, the atom/ion implant 430 will be formed under the Arsenic extension 440, and will have a "lip" formed vertically between the strained silicon channel 450 and the arsenic extension 440. As such, the atom/ion species implant may have an L-shape (in cross section). Thus, at least two sides of the arsenic extension 440 will be surrounded by the atom/ion species implant.

Again, the atom/ion species implanted on the substrate creates vacancy sinks in the vicinity of the arsenic dopant. The presence of the vacancy sinks created by the atom/ion species removes vacancies in the vicinity of the arsenic dopant, thereby retarding (e.g., slowing down) the arsenic diffusion.

Another possible explanation for the mechanism of the present invention is that the atom/ion species may have a binding force to vacancies which is greater than the binding force to vacancies of the dopant. It has also been theorized that the atom/ion species may have a binding force to the dopant which is stronger than the binding force to the dopant of Ge and/or Si atoms. However, these theories should not be considered as limiting the present invention in any manner.

Then, in Figure 4C (and as shown in Figure 4E, in step 430), a spacer 495 is formed, as well as a source/drain implantation is performed, thereby to form the source 496 and drain 497. Thereafter, a source/drain anneal is performed.

It is noted that, in the conventional techniques and devices, typically an anneal is performed after the arsenic implantation step (e.g., after step 410). Thus, in the conventional methods, an extension junction anneal would be performed after the arsenic implantation.

In contrast, the invention does not need to perform an anneal after the arsenic implantation. Instead, the invention may delay the anneal until after the spacer 495 and the source 496/drain 497 implant are in place.

In Figure 4D (and as shown in Figure 4E, in step 440), silicide contacts 498 are formed over the source 496 and drain 497, thereby to complete the device.

Thus, ultra-shallow junctions (e.g., sub-30 nm junctions) can be formed with this exemplary technique of the present invention. It is noted that, while steps may not be necessarily saved by the present invention in view of the conventional techniques, there are no additional steps needed to obtain such ultra-shallow junctions and the invention provides a very convenient method (e.g., not costly) to obtain the ultra-shallow junctions.

It is noted that, in some conventional techniques, some implant patterns may use co-implants in which implants are performed one after another (e.g., in sequence).

However, the invention differs considerably from these techniques in that ultra-shallow junctions (e.g., about 20 nm thickness) having a good slope (e.g., about 5nm per decade of change in concentration of dopant) can be formed, and also such implants of the invention are being performed in strained silicon (or silicon).

It is noted that the invention is applicable to a large range of Ge composition for the $Si_{1-x}Ge_x$ layer (e.g., about x=0.14 to about x=0.75).

Second Exemplary Technique

Figures 5A-5D illustrate processing steps of a second exemplary technique of forming a CMOS (e.g., NMOS) device according to the present

invention. Figure 5E illustrates a flowchart 500 of the exemplary technique of Figure 5A-5D.

The second exemplary technique is similar to the first exemplary technique (e.g., of Figures 4A-4D) except that the first and second steps of the first technique are reversed.

That is, as illustrated exemplary in Figure 5B, first the atom/ion species (e.g., Xe, Si, etc.) is implanted.

Then in step 520 and as shown in Figure 5B, an arsenic extension junction 540 region of the NMOS device in strained $Si/Si_{1-x}Ge_x$ substrates.

Then, similarly to step 430, in Figure 5C (and as shown in Figure 5E, in step 530), a spacer 595 is formed, as well as a source/drain implantation is performed, thereby to form the source 596 and drain 597. Thereafter, a source/drain anneal is performed.

Similarly to Figure 4D and step 440 in Figure 4, in Figure 5D (and as shown in Figure 5E, in step 540), contacts 598 are formed over the source 596 and drain 597, thereby to complete the device.

Thus, again, the second technique is similar to the first technique, except that the order of the arsenic implant and the second species implant is reversed. Thus, the designer would have some flexibility in forming the ultra-shallow junctions.

It is noted that, after step 510 (e.g., performing the atom/ion species implantation) and before step 520 of forming the As extension implant, an anneal could be optionally performed immediately thereafter to remove the

damage created by the species implantation. Such an anneal could be a relatively high temperature anneal (e.g., a rapid thermal anneal performed between about 950 °C to about 1100 °C for a suitable time such as up to about 5 seconds) since the junction has not yet been formed. Thereafter, steps 520 and so forth could be performed (including performing a final source/drain anneal).

Third Exemplary Technique

Figures 6A-6D illustrate processing steps of a third exemplary technique of forming a CMOS (e.g., NMOS) device according to the present invention. Figure 6E illustrates a flowchart 600 of the exemplary technique of Figures 6A-6D.

The third exemplary technique is somewhat similar to the first and second techniques, except that the species implant is made to have a somewhat greater thickness and surrounds (e.g., encloses) (e.g., surrounds at least a portion of) the source and drain region and the arsenic implant extension.

First, in Figure 6A and as shown in Figure 6E, in step 610, an arsenic extension implant 640 is formed. As shown, the implant 640 is formed in a structure 600 somewhat similar to structure 200 shown in Figure 2.

That is, structure 600 includes a substrate 610 (e.g., preferably formed of silicon, silicon-on-insulator, or the like), and a relaxed Si_{1-x}/Ge_x layer 620 formed over (e.g., on top of) the Substrate 610. The Si/Ge layer 620 is a

graded layer which has a crystal lattice which is more and more relaxed in a direction away from a top surface of the substrate 610.

A strained silicon channel 650 is formed between opposing side surfaces of adjacent arsenic extensions 640.

A gate 670 (e.g., formed of polysilicon, metal or the like) is formed above the stained silicon channel 650. A gate oxide 660 is formed between the gate 670 and the channel 650. A shallow trench isolation (STI) 690, formed of dielectric or the like, is formed between devices, adjacent the source and drain.

As illustrated exemplarily in Figure 6B (and as shown in Figure 6E, in step 620), after the implant of arsenic dopants in the extension regions 640, the atom/ion species (e.g., Xe, Si, etc.) is implanted around (e.g., around at least a portion of) the arsenic extension junction 640 region of the NMOS device in strained $Si/Si_{1-x}Ge_x$ substrates.

Then, in Figure 6C (and as shown in Figure 6E, in step 630), a spacer 695 is formed, as well as a source/drain implantation is performed, thereby to form the source 696 and drain 697. Thereafter, a source/drain anneal is performed.

It is noted that the atom/ion species implant surrounds/encloses (e.g., surrounds at least a portion of) the extension and the source/drain regions. That is, the extension is an arsenic implant, and the source/drain is an arsenic implant as well. This means that one obtains enhanced arsenic diffusion from both the extension implant and the source/drain region implant. Thus, arsenic

ions can diffuse into the channel area or even the source/drain can diffuse very fast so as to initially overshadow the extension.

If the species implant is relatively deep, then one can stop the arsenic diffusion in the source/drain region and the arsenic diffusion in the arsenic extension by surrounding (e.g., surrounding at least a portion of) the same with the species implant, thereby providing more control. Thus, in contrast to the first and second exemplary techniques, the third technique can slow down the arsenic diffusion in both the arsenic extension and the source/drain, thereby providing a better device.

As shown in Figure 3A, it can be clearly seen that the source/drain is deeper than the species implant, as compared to the structure of Figure 6A where the source/drain (and arsenic extension) are surrounded (e.g., at least a portion are surrounded) by the species implant.

In Figure 6D (and as shown in Figure 6E, in step 640), contacts 698 are formed over the source 696 and drain 697, thereby to complete the device.

Fourth Exemplary Technique

Figures 7A-7D illustrate processing steps of a fourth exemplary technique of forming a CMOS (e.g., NMOS) device according to the present invention. Figure 7E illustrates a flowchart 700 of the exemplary technique of Figures 7A-7D.

This exemplary technique is similar to the first technique (e.g., shown in Figures 4A-4D), except that a different formation sequence is employed,

That is, a disposable spacer is used as an implant mask in forming the source/drain, and the order of forming the source/drain is reversed from that of the previous techniques. Thus, the source/drain is formed first in the fourth exemplary technique, followed by forming the Arsenic extension, the species implant, the spacer formation, and the silicide contacts.

First, in Figure 7A and as shown in Figure 7E, in step 710, a disposable spacer 795A is formed adjacent a gate 770.

That is, the structure of Figure 7A includes a substrate 710 (e.g., preferably formed of silicon, silicon-on-insulator, or the like), a relaxed Si_{1-x}/Ge_x layer 720 formed over (e.g., on top of) the substrate 710. The Si/Ge layer 720 preferably is a graded layer which has a crystal lattice which is more and more relaxed in a direction away from a top surface of the substrate 710.

A strained silicon channel 750 is formed underneath the gate 770.

The gate 770 (e.g., formed of polysilicon, metal or the like) is formed above a stained silicon channel 750. A gate oxide 760 is formed between the gate 770 and the channel 750. A shallow trench isolation (STI) 790, formed of dielectric or the like, is formed between devices.

The disposable spacer 795A is for forming the source/drain, and will mask the area where the arsenic junction extension will be formed.

As illustrated in Figure 7B (and step 720 of Figure 7G), the source 796/drain 797 junction is formed.

In Figure 7C (and step 730 of Figure 7G), the disposable spacer 795A is removed, and the extension junction implant is formed (e.g., with Arsenic) for forming the extension regions 740.

As illustrated exemplary in Figure 7D, after the removal of the disposable spacer 795A and the implant of arsenic dopants in the extension regions 740, the atom/ion species (e.g., Xe, Si, etc.) are implanted around the arsenic extension junction 740 region of the NMOS device in strained $Si/Si_{1-x}Ge_x$ substrates.

In Figure 7D (and as shown in Figure 7E, in step 740), the species (e.g., Xe, Ge, Si, Ar, Kr, Ne, He and N) implant 730 is formed.

Then, in Figure 7E (and as shown in Figure 7G, in step 750), a spacer 795B is formed, as well as a source/drain implantation is performed, thereby to form the source 796 and drain 797. Thereafter, a source/drain anneal is performed.

In Figure 7F (and as shown in Figure 7G, in step 760), contacts 798 are formed over the source 796 and drain 797, thereby to complete the device.

It is noted that processing similar to the third exemplary technique (e.g., as shown in Figures 6A-6D) could be employed in which the atom/ion species implant could be performed relatively deep, so as to surround/enclose (e.g., surround at least a portion of) the extension and the source/drain region.

Thus, with the techniques of the invention, ultra-shallow junctions can be formed in strained silicon (or silicon) which have not been achievable prior to the present invention.

While the invention has been described in terms of several exemplary embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

Further, it is noted that, Applicant's intent is to encompass equivalents of all claim elements, even if amended later during prosecution.